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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/343,872	06/30/1999	TUAN Q. DAO	5201-20400	8423

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LSI LOGIC CORPORATION  
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EXAMINER
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HUYNH, KIM T

ART UNIT	PAPER NUMBER
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2112

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12

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/343,872	Applicant(s) DAO ET AL.	
	Examiner Kim T. Huynh	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-8 and 10-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8 and 10-24 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 June 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### ***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 3-8, 10-12, 14-17, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (Pub No US20020002662) in view of Sudo (US Patent 6,298,384)

As per claim 1, Olarig discloses a data transfer apparatus that comprises:

- A plurality of busses each configured to couple a processing device to a corresponding memory module; [0134-0136]
- At least one cross-bus coupled to each of the plurality of busses by one or more bus bridges, wherein the bus bridges each include a set of multiplexers 720 that are configurable to steer signals from the bus to the cross-bus, and are further configurable to steer signals from the cross-bus to the bus; and [0134-0138]
- A memory management unit 200 configured to receive memory access requests from a plurality of processing devices and to responsively configure the bus bridges to steer address and data signals accordingly, [0013], [0040]

- Wherein the plurality of busses includes two bit lines for each data bit and the at least one cross-bus includes two unidirectional bit lines for each data bit, and wherein the bus bridges include a multiplexer for each outgoing bit line that selects from three other incoming bit lines. [0074-0076]

Olarig discloses all the limitations as above but not explicitly discloses unidirectional bit lines. However, Sudo discloses a switch 43 for switching between the unidirectional buses, a CPU for providing controls over, ie, data processing in the module itself, and a shared memory allowing access not only from a CPU in the module but also from CPUs of other modules. (col.6, lines 6, lines 5-9)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Sudo's teaching into Olarig's system so as the data transfer capability can be improved with a low cost configuration for upgrading performance of the system as a whole. (col.3, lines 7-13)

As per claim 11, Olarig discloses a method for transferring data between a set of memory modules and a set of processor units, wherein the method comprises:

- Said processing units providing transfer requests to a memory manager; [0040]

- Said memory manager setting a router in a conflict-free access pattern in response to said transfer requests, wherein setting said router includes; [0137], [0142]
- Said memory manager providing control signals to bus bridges that couple local busses between a memory module and a processing device to a cross-bus between the local busses, [0134-0137]
- Wherein the local busses each include two bit lines for each data bit and the cross-bus includes two bit lines for each data bit, wherein the bus bridges each include a multiplexer for each outgoing bit line that selects from multiple incoming bit lines; and [0074-0076]
- Said processing units accessing memory modules via said router. [0136-138]

Olorig discloses all the limitations as above but not explicitly discloses unidirectional bit lines. However, Sudo discloses a switch 43 for switching between the unidirectional buses, a CPU for providing controls over, ie, data processing in the module itself, and a shared memory allowing access not only from a CPU in the module but also from CPUs of other modules. (col.6, lines 6, lines 5-9)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Sudo's teaching into Olorig's system so as the data transfer capability can be improved with a

low cost configuration for upgrading performance of the system as a whole. (col.3, lines 7-13)

As per claim 16, Olarig discloses a high-bandwidth bus system which comprises:

- A plurality of local memory busses each for transferring data between a processing device and an associated memory module;[0136-0138]
- One or more local intersect busses for transferring data between the plurality of local memory busses, wherein said local intersect busses are coupled to each of the plurality of local memory busses by four multiplexers at each intersection; and [0134-0138]
- A memory controller 200 means for setting each multiplexer to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules, [142]
- Wherein the local memory busses each include two bit lines for each data bit and local intersect busses includes two bit lines for each data bit.[0074-0076]

Olarig discloses all the limitations as above but not explicitly discloses unidirectional bit lines. However, Sudo discloses a switch 43 for switching between the unidirectional buses, a CPU for providing controls over, ie, data processing in the module itself, and a shared memory allowing access not only from a CPU in the module but also from CPUs of other modules. (col.6, lines 6, lines 5-9)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Sudo's teaching into Olarig's system so as the data transfer capability can be improved with a low cost configuration for upgrading performance of the system as a whole. (col.3, lines 7-13)

As per claim 3, Olarig discloses wherein the memory management unit includes an interrupt controller 190 configurable to assert an interrupt signal to said processing devices after completing a block transfer of data. [0137-139]

As per claims, 4-6, 14, 19-22, Olarig discloses wherein the memory management unit includes one or more request queues, wherein said one or more request queues includes a single transfer queue configured to store access requests relating to single data word, block data, message transfers [0142], [0013], wherein identify requests, ie memory access parameters inherently discloses type of data transfer)

As per claims 7, 23, Olarig discloses wherein the memory management unit includes an interrupt controller configurable to assert an interrupt signal to a processing device that is an addressee of a message transfer request. [0137-0138]

As per claims 8, 24, Olarig discloses the data transfer further comprising port logic connected to the plurality of busses and configured to couple to the processing devices, wherein the port logic is further coupled to the memory

management unit and configured to prevent writes to protected memory. Fig.10,  
[0074-0076]

As per claim 10, Olarig discloses wherein said plurality of busses includes at least three busses. [0134-0136]

As per claim 12, Olarig discloses wherein before setting said router, said memory manager determines said conflict-free access pattern in accordance with assigned priorities for each transfer request. [0142]

As per claim 15, Olarig discloses a high-bandwidth bus which comprises

- A plurality of local busses each for transferring data between a processing device and an associated memory module;[0136-0138]
- A cross-bus for transferring data among the plurality of local busses, wherein said cross-bus is coupled to each of the plurality of local busses by a bridge means; and [0134-138]
- A memory controller 200 means for setting said bridge means to provide processing devices with access to memory modules, wherein the memory controller means is configured to provide highest priority for accesses from processing devices to the associated memory modules; [0142]
- Wherein the local busses each include two bit lines for each data bit and the cross-bus includes two unidirectional bit lines for each data bit. [0074-0076]

Olarig discloses all the limitations as above but not explicitly discloses unidirectional bit lines. However, Sudo discloses a switch 43 for



switching between the unidirectional buses, a CPU for providing controls over, ie, data processing in the module itself, and a shared memory allowing access not only from a CPU in the module but also from CPUs of other modules. (col.6, lines 6, lines 5-9)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Sudo's teaching into Olarig's system so as the data transfer capability can be improved with a low cost configuration for upgrading performance of the system as a whole. (col.3, lines 7-13)

As per claim 17, Olarig discloses wherein the four multiplexers forward data between a processing device and a memory device with essentially no latency delay. [0142]

3. Claims 2, 13, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Olarig et al. (Pub No US20020002662) in view of Sudo (US Patent 6,298,384) and further in view of Geiger et al. (Pub No US20020091905)

Olarig discloses all the limitations as above except memory manager operating a direct memory access controller to perform data transferring between memory modules. Whereas, Geiger discloses system 200 is operable to data transferred to/from memory components or devices comprises on the module include DMA controller to move data in the system memory. [0122]

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Geiger's teaching into Olarig's

system so as to have ability to access transferred data independently between modules.

***Response to Amendment***

4. Applicant's amendment filed on 12/19/03 have been fully considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

*Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.*

*If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.*

*Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.*



Kim Huynh

March 9, 2004

**Khanh Dang**  
**Primary Examiner**